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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,707	DORSEY, MICHAEL C.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *4 and 14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-14,15-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 3/5/02 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/26/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to applicant's amendment filed 6/4/2004.

Claims 4 and 14 were cancelled.

Claims 1-3, 5-13 and 15-36 are pending in this action.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 7/26/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

2. The examiner acknowledges and approves the applicant's changes to Figure 9, and the examiner withdraws all objections to said Drawings.

3. The examiner acknowledges and approves the applicant's changes to the Specification, and the examiner withdraws all objections to said Specification.

4. The examiner acknowledges the applicant's changes to Claim 35, and the examiner withdraws the objection to said Claim 35.

Re: 35 USC § 112 Claim Rejections

5. In view of the applicants amendments to Claims 26, 27 and 28, and cancellation of Claims 4 and 14, the examiner withdraws all rejections under 35 USC 112 first and second paragraphs.

Re: 35 USC § 102 and § 103 Claim Rejections

6. Applicant's arguments based on the amendment filed 6/4/2004, with respect to the rejections of independent Claims 1, 7, 11 and 19, anticipated by Motika, and independent Claims 25 and 30, anticipated by Kraus, all under 35 USC § 102, have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. Consequently, the rejections of the dependent claims under the aforementioned independent claims are also withdrawn. In all, the rejections of Claims 1-3, 5-13 and 15-36 are withdrawn. However, upon further consideration, a new grounds of rejection is made in view of the addition of the following limitation to the independent claims: "wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit" (see below).

Claim Rejections - 35 USC § 103

7. Claims 1-3, 7-9, 11-13 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Kohno, U.S. Patent No. 5943285.

As per Claim 1:

Motika et al. teaches a built-in self-test controller (FIG.2 50), comprising: a plurality of alternative memory built-in self-test state machines (FIG.2 32); and a memory built-in self-test engine operating a predetermined one of the memory built-in self-test state machines (FIG.2 32 and column 3 lines 38-63). But, not taught by Motika

et al. is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and column 8 lines 8-27. And in column 1 lines 6-9 and column 5 lines 57-67, the inventor cites advantages of less restricted design requirements while maintaining fast circuit speed. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to apply the centralized theme of Kohno to the controller taught by Au et al. and Motika et al. in order to produce a better self-testing product.

As per Claim 2:

Motika et al. further teaches the built-in self-test controller of claim 1(FIG.2 50), further comprising a logic built-in self-test engine (FIG.2 34). And in view of the motivation previously stated, the claim is rejected.

As per Claim 3:

Motika et al. further teaches the built-in self-test controller of claim 1 (FIG.2 50), further comprising a memory built-in self-test signature generated by an execution of the memory built-in self-test (column 3 lines 56-60). And in view of the motivation previously stated, the claim is rejected.

As per Claim 7:

Motika et al. teaches a built-in self-test controller (FIG.2 50), comprising: means for implementing a plurality of states in a plurality of sets in a memory built-in self-test (column 2 lines 63-65); and means for operating a predetermined one of the sets in the memory built-in self-test (column 4 lines 6-8). But, not taught by Motika et al. is wherein

the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and column 8 lines 8-27. And in view of the motivation previously stated, the claim is rejected.

As per Claim 8:

Motika et al. further teaches the built-in self-test controller of claim 7, further comprising a logic built-in self-test engine (FIG.2 34 and column 3 lines 39-42). And in view of the motivation previously stated, the claim is rejected.

As per Claim 9:

Motika et al. further teaches the built-in self-test controller of claim 7, further comprising a memory built-in self-test signature generated by an execution of the memory built-in self-test (column 3 lines 5660). And in view of the motivation previously stated, the claim is rejected.

As per Claim 11:

Motika et al. teaches an integrated circuit device (column 1 lines 5-9), comprising: a plurality of memory components (FIG.2 36); a testing interface (FIG.2 60), and a built-in self-test controller controlled through the testing interface (FIG.2 50), comprising: a plurality of alternative memory built-in self-test state machines (FIG.2 32); and a memory built-in self-test engine (FIG.2 32) operating a predetermined one of the memory built-in self-test state machines. But, not taught by Motika et al. is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and

column 8 lines 8-27. And in view of the motivation previously stated, the claim is rejected.

As per Claim 12:

Motika et al. further teaches the integrated circuit device of claim 11, further comprising a logic built-in self-test engine (FIG.2 34). And in view of the motivation previously stated, the claim is rejected.

As per Claim 13:

Motika et al. further teaches the integrated circuit device of claim 11, further comprising a memory built-in self-test signature register generated by an execution of the memory built-in self-test (column 3 lines 56-60). And in view of the motivation previously stated, the claim is rejected.

As per Claim 19:

Motika et al. teaches an integrated circuit device (column 1 lines 5-9), comprising: a plurality of memory components (FIG.2 36); a testing interface (FIG.2 60); and a built-in self-test controller controlled through the testing interface (FIG.2 50), comprising: means for implementing a plurality of states in a plurality of sets in a memory built-in self-test (FIG.2 32 and column 4 lines 6-8); and means for operating a predetermined one of the sets in the memory built-in self-test (column 4 lines 6-8). But, not taught by Motika et al. is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and column 8 lines 8-27. And in view of the motivation previously stated, the claim is rejected.

As per Claim 20:

Motika et al.further teaches the integrated circuit device of claim 19, further comprising a logic built-in self-test engine (FIG.2 34). And in view of the motivation previously stated, the claim is rejected.

As per Claim 21:

Motika et al. further teaches the integrated circuit device of claim 19, further comprising a memory built-in self-test signature register generated by an execution of the memory built-in self-test (column 3 lines 53-60). And in view of the motivation previously stated, the claim is rejected.

8. Claims 25, 29, 30 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., U.S. Patent No. 6587979, and in view of Kohno, U.S. Patent No. 5943285.

As per Claim 25:

Kraus et al. teaches a feature for performing a built-in self-test on an integrated circuit device (see Abstract), comprising: externally resetting a predetermined one of a plurality of memory state machines in a memory built-in self-test controller (column 9 lines 52-58); performing a memory built-in self-test utilizing the reset memory state machine (column 9 lines 58-67); and obtaining the results of the performed memory built-in self-test (column 10 lines 55-61). But, not taught by Kraus et al. is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and

column 8 lines 8-27. And in view of the motivation previously stated, the claim is rejected.

As per Claim 29:

Kraus et al. further teaches the feature of claim 25, wherein obtaining the results includes receiving the results as the memory built-in self-test is performed (column 10 lines 61-67). And in view of the motivation previously stated, the claim is rejected.

As per Claim 30;

Kraus et al. teaches a feature for testing an integrated circuit device (see Abstract), comprising: interfacing the integrated circuit device with a tester (column 9 lines 24-26 and FIG.5 21); externally resetting a built-in self-test controller (column 9 lines 52-58), including: externally resetting a predetermined one of a plurality of memory state machines (column 9 lines 52-67); performing a memory built-in self-test from the built-in self-test controller (column 9 lines 52-67 and column 10 lines 1-3); obtaining the results of the performed memory built-in self-test (column 10 lines 55-61). But, not taught by Kraus et al. is wherein the dual-mode built-in self-test controller is geographically centralized within an integrated circuit. But in an analogous art, Kohno does teach this feature (see Abstract, and column 8 lines 8-27. And in view of the motivation previously stated, the claim is rejected.

As per Claim 36:

Kraus et al. further teaches the feature of claim 30, wherein obtaining the results includes receiving the results as the memory built-in self-test is performed(column 10 lines 61-67). And in view of the motivation previously stated, the claim is rejected.

9. Claims 5, 15, 18 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, in view of Kohno, U.S. Patent No. 5943285 as applied to claim 3, 11 and 13 above, and further in view of Au et al., U.S. Patent No. 6681359.

As per Claims 5 and 15:

The controller of Claim 3 or 13 is further limited whereas the signature includes a "done" bit. But Motika et al. and Kohno et al. fail to teach this feature. Au et al., in column 9 line 25-33 defines such a feature. And Au et al., in column 2 lines 18-27 in reciting the attributes of the invention, boasts of a better means to retrieve information within an MBIST while not requiring a large number of device pins. One with ordinary skill in the art at the time of the invention, motivated by Au et al., would combine the two references, thus the claims are rejected.

As per Claim 18 and 24:

The device of Claim 11 or 19 is further limited whereas the interface is a JTAG tap controller. Au et al., in FIG.3 112 and in the Abstract teaches such an arrangement, and in view of the motivation for Au et al. elsewhere, the claim is rejected.

10. Claims 17 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, in view of Kohno, U.S. Patent No. 5943285 as applied to Claims 11 and 19 above, and further in view of Kim et al., U.S. Patent No. 6148426. In view of the failure to disclose an MBIST, by Motika et al. and Kohno et al., in an analogous art, Kim et al. teaches an MBIST (see Abstract) that is used for testing an SRAM (see Title). Citing a savings in BIST size and cost (column 2 lines 55-61), Kim

et al. would motivate one with ordinary skill in the art at the time of the invention to combine the teaching of Kim et al. with Motika et al. and Kohno et al. for the purpose of testing SRAM memories.

11. Claims 6, 10, 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Kohno, U.S. Patent No. 5943285 as applied to claims 1 and 7 and 11 and 19 above, in view of Zuraski Jr. et al., U.S. Patent No. 6560740, and further in view of Lo et al., U.S. Patent No. 5661732. The claims, dependent on Claim 1 or 7 or 11 or 19 above, further limit the controller wherein the state machine comprises a reset state entered upon an external reset signal (Zuraski et al, column 10 lines 31-36). However Zuraski et al. does not further limit the machine to flushing and testing. In an analogous art, Lo et al., upon entering a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), the next state produces internal resets of registers, and then as a programmable option, a flush of the memory may occur (Lo et al. column 13 lines 6-10) and then subsequent testing (same reference) may take place. At the end of the test, a state described by column 5 lines 17-35 occurs with the initiation of a test done signal (Lo et al. FIG.1 26). In Zuraski et al., a better BIST for functionally testing memories is discussed, and in Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. One with ordinary skill in the art at the time of the invention, motivated by Zuraski et al. and Lo et al., would combine the references, and so the claims are rejected.

12. Claims 26, 27, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., U.S. Patent No. 6587979, in view of Kohno, U.S. Patent No. 5943285 as applied to claims 25 and 30, and further in view of Lo et al., U.S. Patent No. 5661732.

As per Claims 26 and 31:

The claims, dependent on Claims 25 or 30 above, further limit the features wherein a state is entered upon to initialize the MBIST. In an analogous art, Lo et al., upon entering a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), the next state produces internal resets of registers, and then as a programmable option, a flush of the memory may occur (Lo et al. column 13 lines 6-10) and then subsequent testing (same reference) may take place. At the end of the test, a state described by column 5 lines 17-35 occurs with the initiation of a test done signal (Lo et al. FIG.1 26). One with ordinary skill in the art at the time of the invention, motivated by Lo et al. as previously stated, would combine the references, and so the claims are rejected.

As per Claims 27 and 32:

The claims, dependent on Claims 26 and 31above, further limit the features to storing the results in a MBIST signature register, and setting a bit in the MBIST signature register indication that the test is done (Kraus et al. column 10 lines 55-61). Therefore, in view of the prior motivation, the claims are rejected.

13. Claims 28 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., U.S. Patent No. 6587979, in view of Kohno, U.S. Patent No. 5943285

as applied to Claims 25 and 30 above, and further in view of Motika et al., U.S. Patent No. 5982189.

As per Claim 28:

The feature of Claim 25 is further limited wherein the external reset of Kraus et al. (column 9 lines 52-58) is performed on the logic machine. In an analogous art, Motika et al. performs an LBIST and then obtains the results (column 3 lines 64-67 and column 4 lines 1-5). And whereas one with ordinary skill in the art at the time of the invention, motivated to perform a BIST with built-in stress testing (Motika et al., column 1 lines 64-67), would combine the references for this purpose, thus the claim is rejected.

As per Claim 33:

The feature of Claim 30 is further limited wherein obtaining the results includes reading a signature register. Motika et al., in column 3 lines 56-60 supports such a feature, and in view of the prior motivation for Motika et al., the claim is rejected.

14. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., U.S. Patent No. 6587979, in view of Kohno, U.S. Patent No. 5943285 as applied to claim 30 above, and in view of Au et al., U.S. Patent No. 6681359. The feature of Claim 30 is further limited whereas the interface is a JTAG tap controller. Au et al., in FIG.3 112 and in the Abstract teaches such an arrangement, and in view of the motivation for Au et al. elsewhere, the claim is rejected.

15. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kraus et al., U.S. Patent No. 6587979 , in view of Kohno, U.S. Patent No. 5943285 as applied to claim 30 above, and in view of Arimilli et al., U.S. Patent No. 6665828. The feature of

Claim 30 is further limited whereas the resetting of the BIST includes resetting an LBIST, further performing an MBIST. Kraus et al. performs the MBIST as per Claim 30, but does not reset an LBIST. In an analogous art, Arimilli et al. in column 6 lines 7-31 performs such a task. And, as Arimilli et al. describes a better way to test ever-larger circuits without increasing test circuit size (column 1 lines 1-67 and column 2 lines 1-6), one with ordinary skill in the art at the time of the invention, motivated by Arimilli et al., would combine the references, and so the claim is rejected.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 571-272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
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Guy J. LAMARRE
PRIMARY EXAMINER